Characterization of Si/SiGe Heterostructures for Strained Si CMOS

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Outline

- Introduction
    - why strained Si devices?

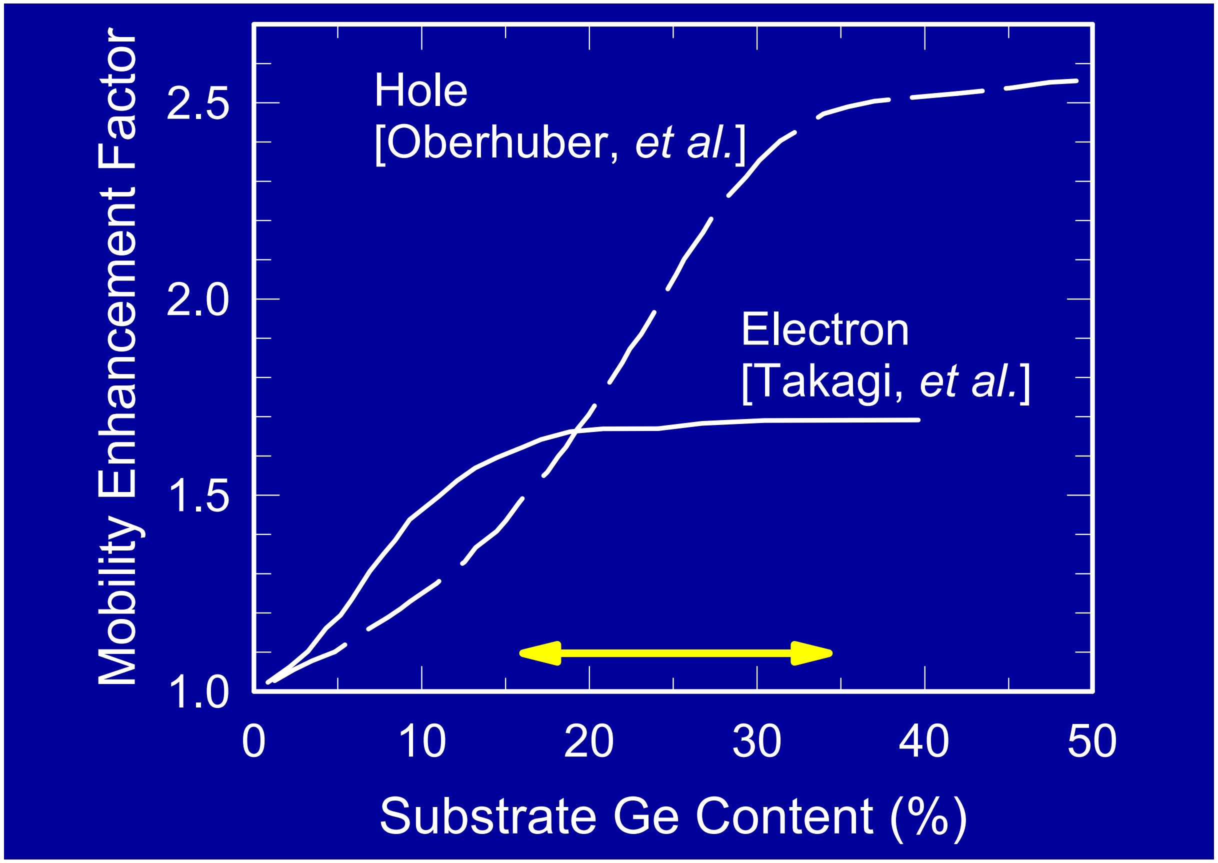
- Layer structures for strained Si CMOS
    - graded buffer layers
    - alternative approaches to relaxed SiGe
    - SiGe-on-insulater and strained Si-on-insulator

- Nondestructive characterization of strained Si-on-SiGe structures
    - thermal stability of strained Si on SiGe

- Conclusions

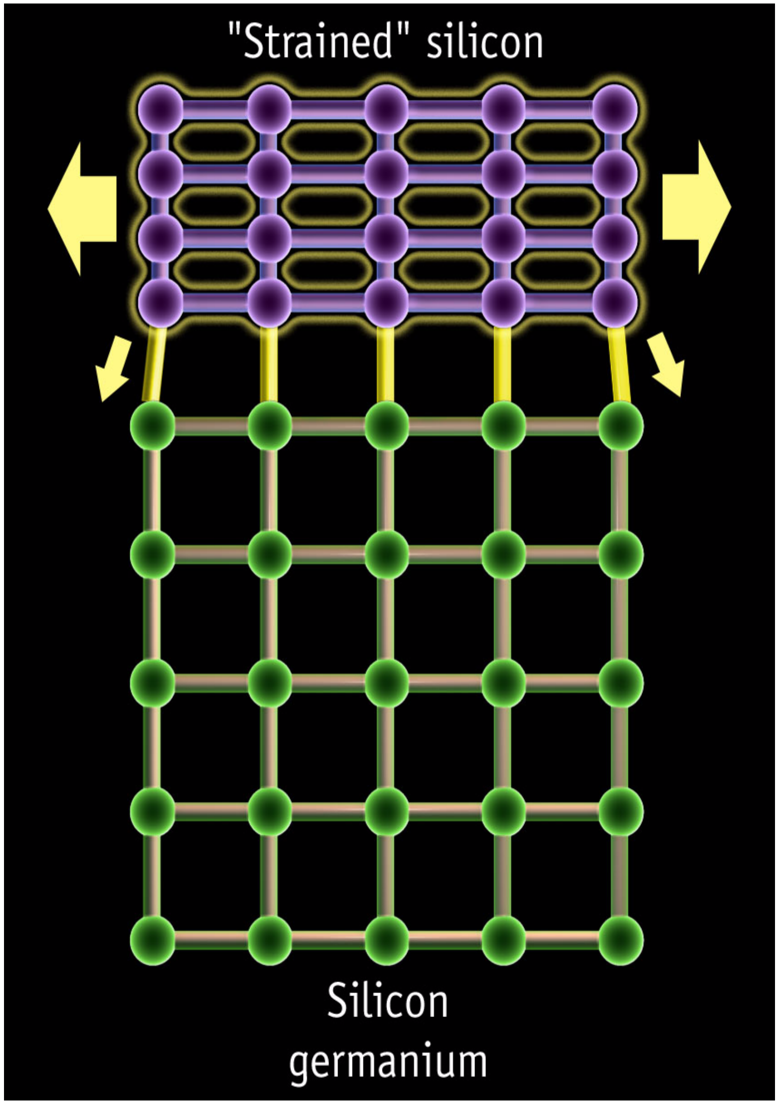
Strained Si Device Structures

modified band structure of Si under biaxial tensile strain ==> enhanced mobility

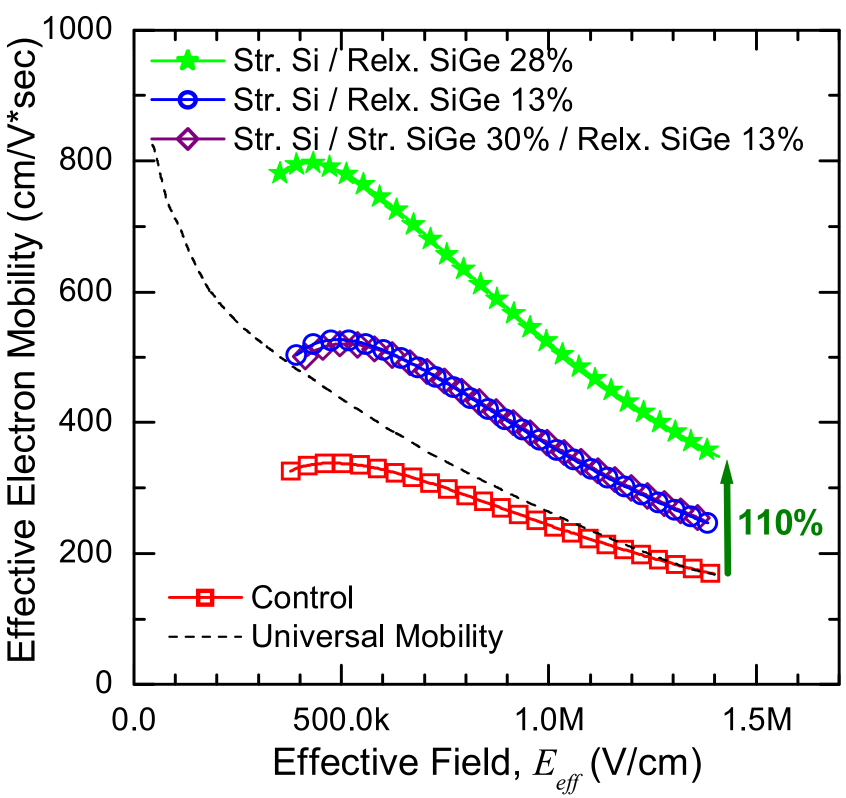


need relaxed $Si_{1-x}Ge_x$ with $0.15<x<0.35$

Strained Si on SiGe



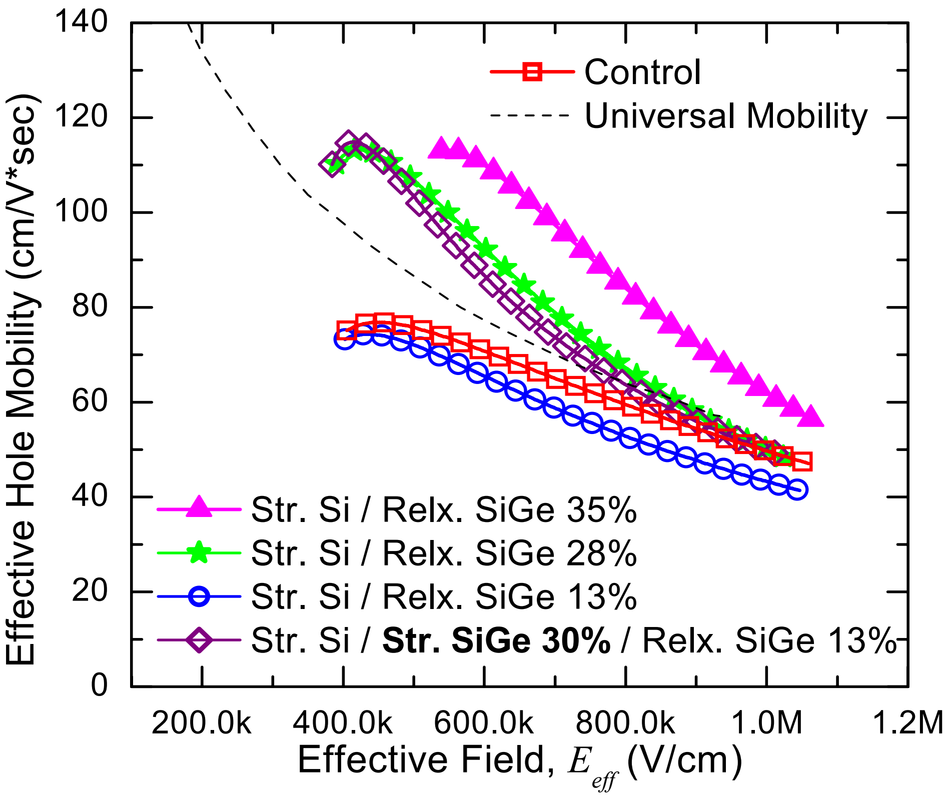
Enhanced Mobility in Strained Si Devices



electron mobility is

- 70% higher in $Si_{0.87}Ge_{0.13}$
- 110% higher in $Si_{0.72}Ge_{0.28}$

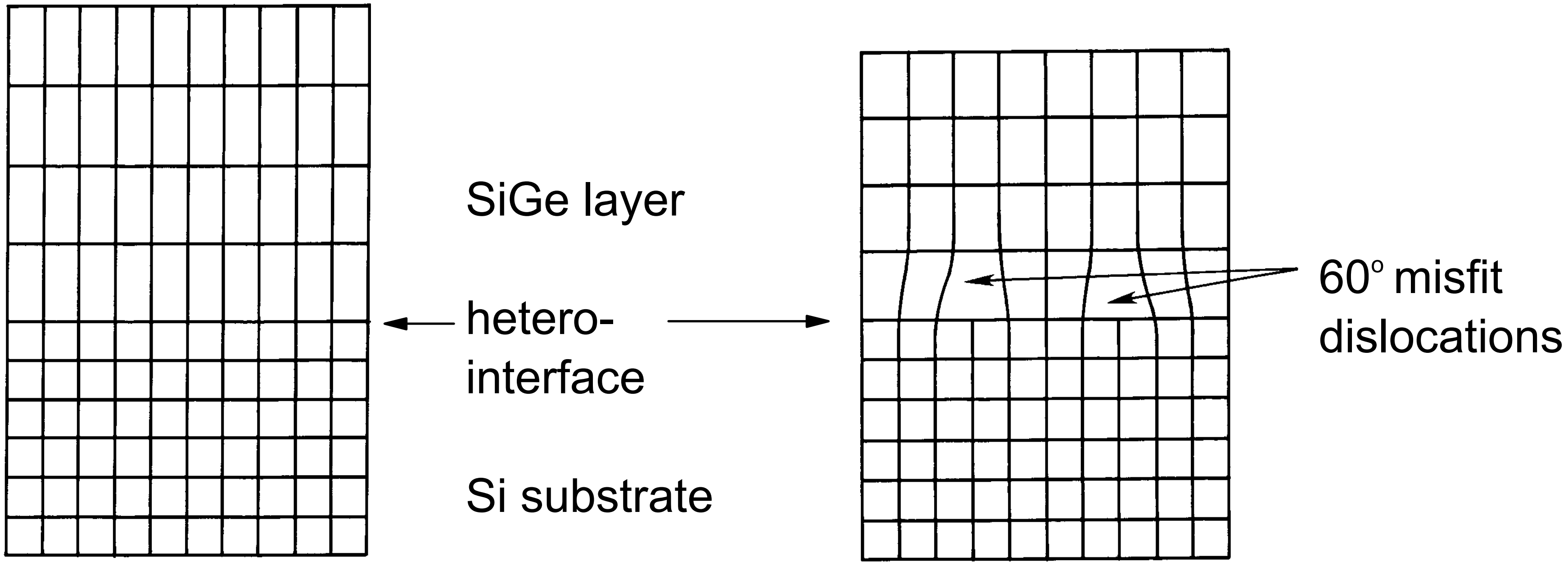
higher than theory predicted!



peak hole mobility is enhanced in $Si_{0.72}Ge_{0.28}$ and $Si_{0.65}Ge_{0.35}$ but decreases at higher electric field

K. Rim, et al., ISTDM, Nagoya, Japan, January 15-17, 2003

Epitaxial SiGe Layers on Si(001)



SiGe layer

hetero-interface

Si substrate

60° misfit dislocations

Pseudomorphic layer:

in-plane: $a_{\parallel} = a_{Si}$

out-of-plane: $a_{\perp} > a_{SiGe}$

Partially relaxed layer:

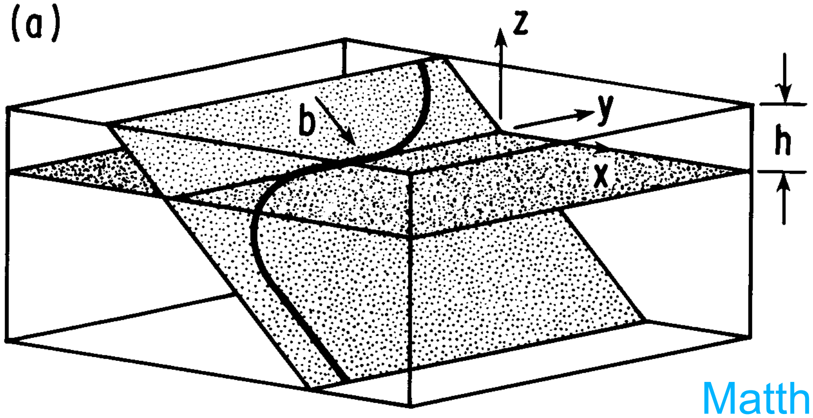
$a_{Si} < a_{\parallel} < a_{SiGe}$

$a_{\perp} > a_{SiGe}$

100% relaxed layer:

$a_{\parallel} = a_{\perp} = a_{SiGe}$

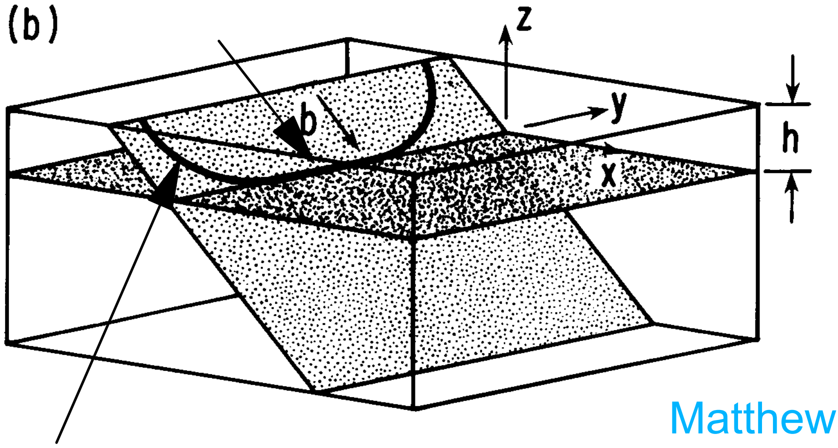
Strain Relaxation via 60° Misfit Dislocations



misfit segment formed by glide of an existing dislocation

e.g. Si on relaxed SiGe

Matthews, et al., Thin Solid Films 33, 253 (1976).



misfit segment

threading arm

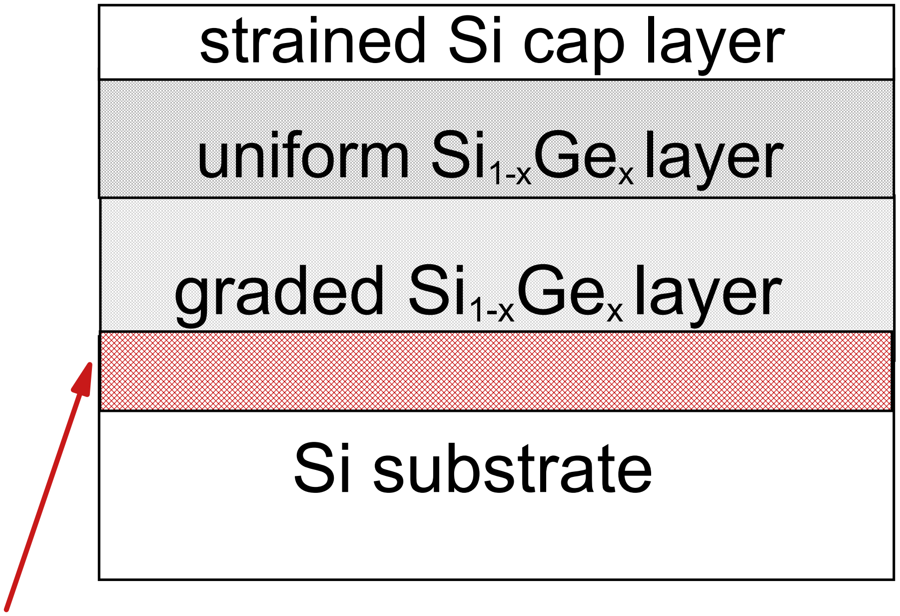
nucleation of a dislocation during epitaxial growth

e.g. SiGe on Si substrates

Matthews & Blakeslee, J. Cryst. Growth 32, 265 (1976).

must minimize threading dislocation density for devices!

Compositionally Graded SiGe Buffer Layers for Devices



strained Si cap layer

uniform $Si_{1-x}Ge_x$ layer

graded $Si_{1-x}Ge_x$ layer

Si substrate

misfit dislocation network buried below devices

advantages:

low threading dislocation densities (10^5-10^8 cm^{-2})

lower grading rates (thicker layers)
==> lower defect density

disadvantages:

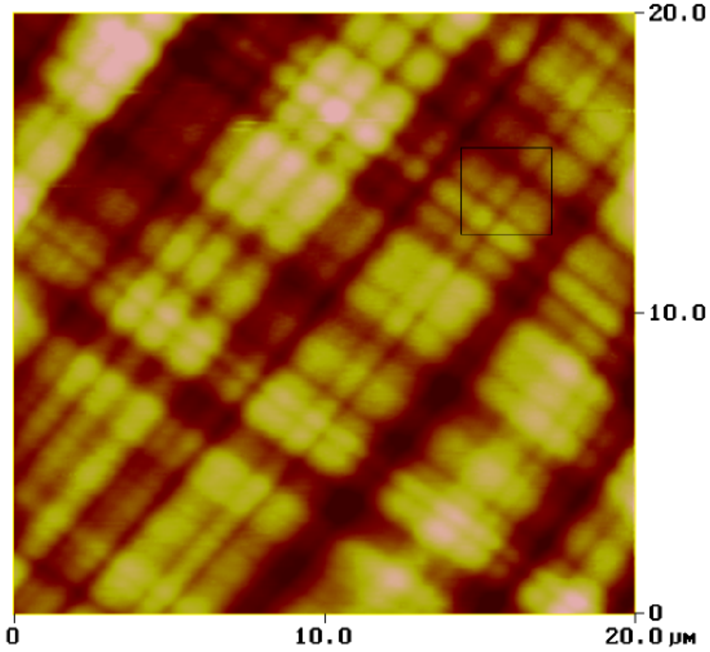
very thick SiGe layers (1-4 μm)

- expensive
- poor heat conductivity

rough surface (cross hatch)

- can polish surface (CMP)

inhomogeneous distribution of threading dislocations



20μm x 20μm -- $Si_{0.85}Ge_{0.15}$
z-range = 40nm, RMS = 6nm

Thin Relaxed SiGe Layers on Si(001)

Alternatives to thick graded buffer layers:

-- Grow Si layer at low temperature underneath SiGe (MBE)

"compliant layer" - high density of point defects in LT Si layer

- M. Bauer, et al., Thin Solid Films 369, 152 (2000).

-- Ion implantation of H or He

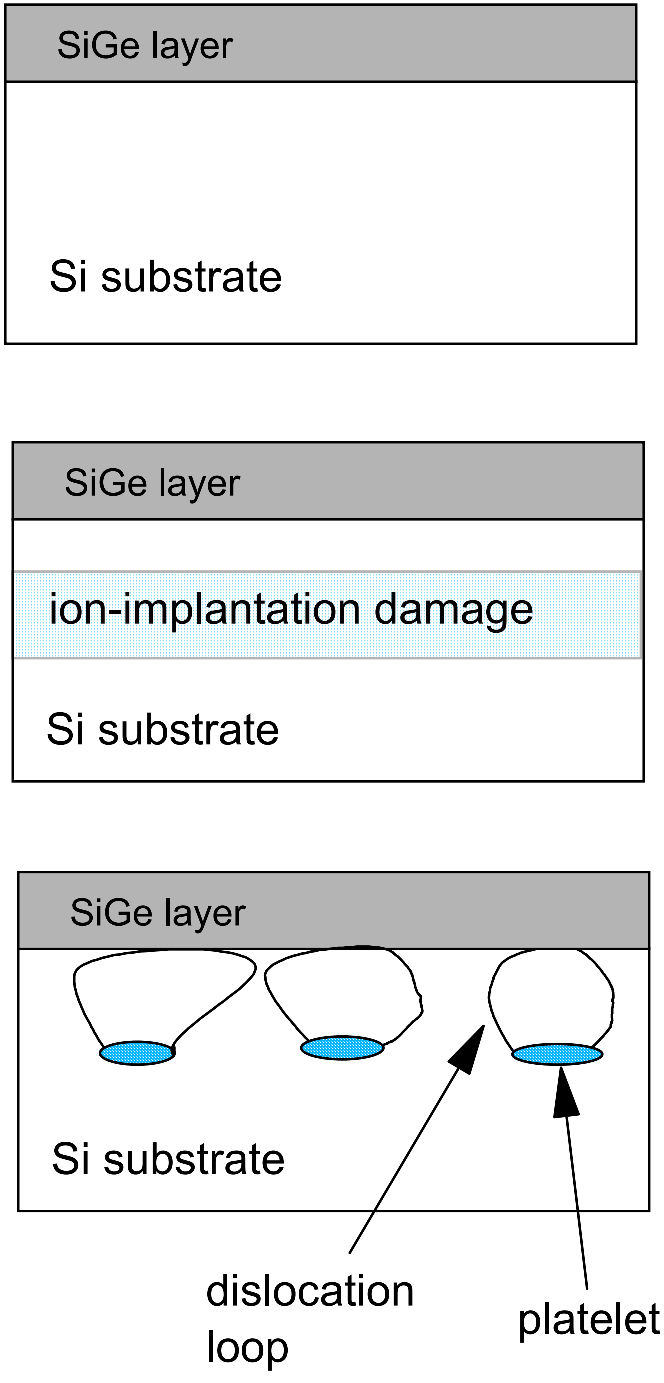
extended defects (bubbles) formed during high temperature annealing in implanted wafer act as nucleation sources for dislocations

- D.M. Follstaedt, et al., Appl. Phys. Lett. 69, 2059 (1996).
- S. Mantl, et al., Nucl. Instr. and Meth. B147, 29 (1999).
- M. Luysberg, et al., J. Appl. Phys. 92, 4290 (2002).
- S.H. Christiansen, et al., Mat. Res. Soc. Symp. Proc. **686**, 27 (2002).

Ion Implanted/Annealed Relaxed SiGe Buffer Layers

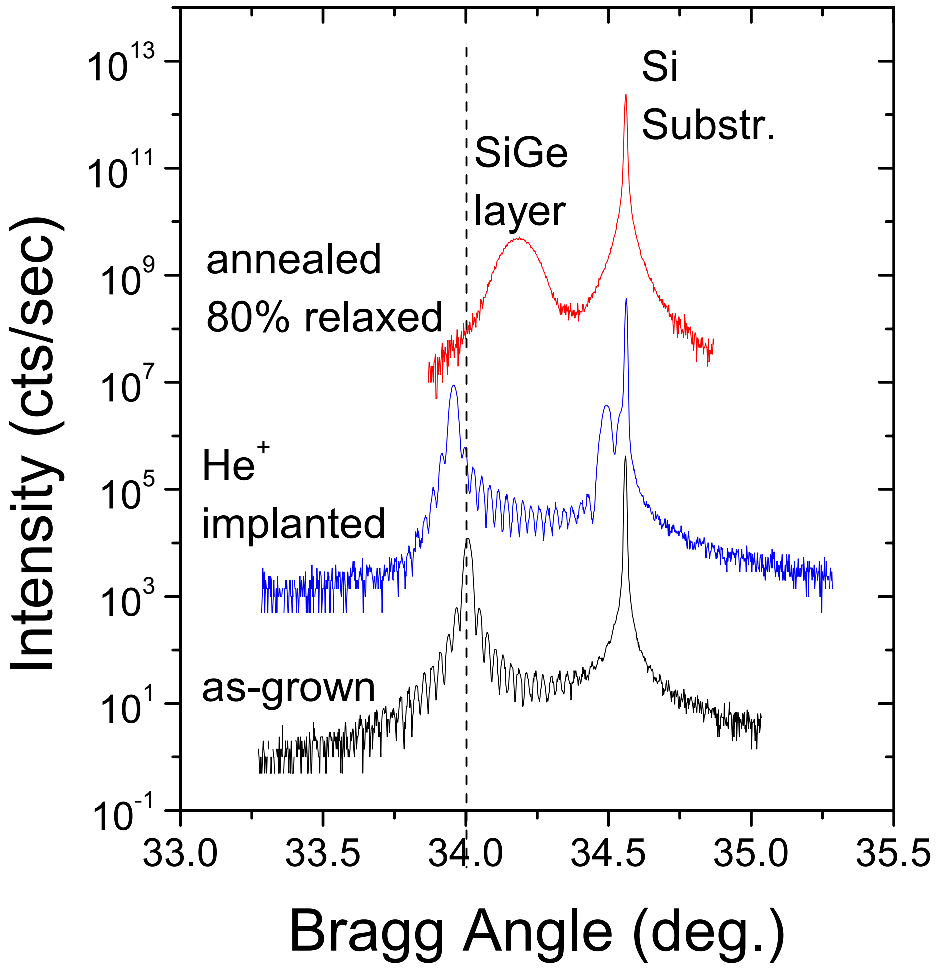
3 step process:

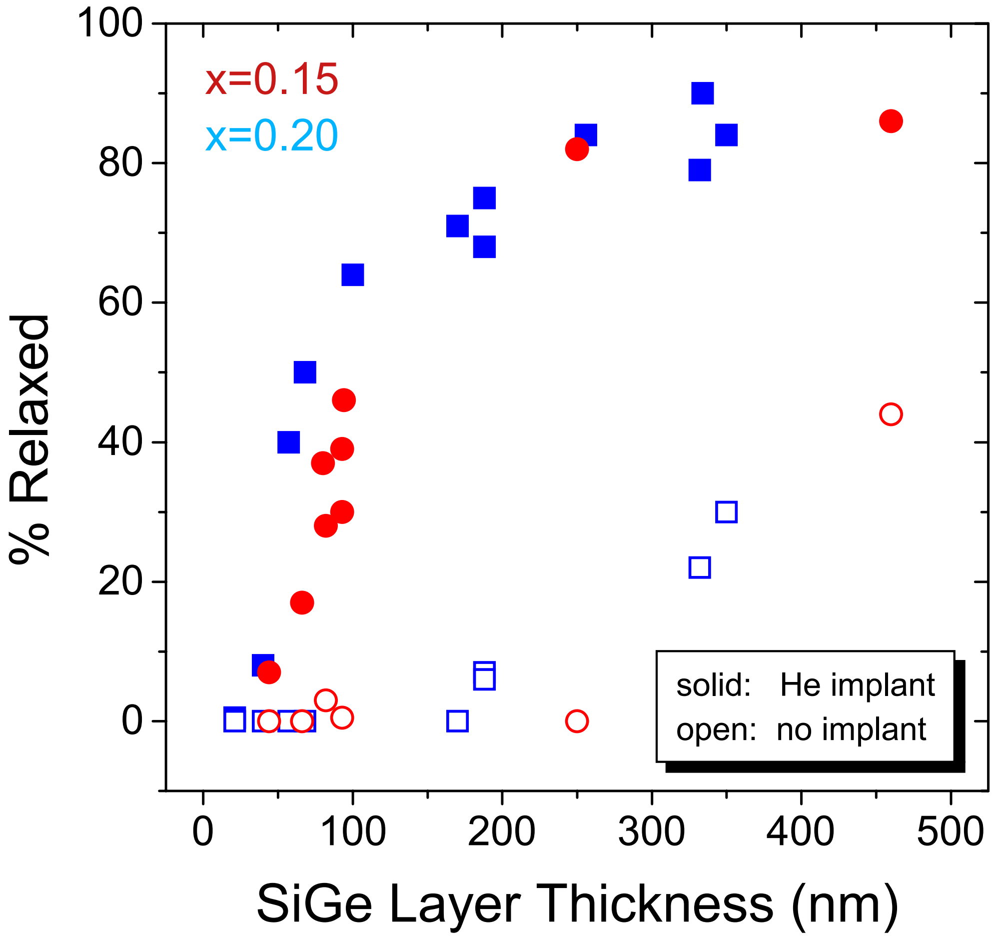
- grow 50-300 nm pseudomorphic (fully strained) SiGe layer on Si
- implant He^+ at various doses and energies, R_p at or below SiGe/Si interface
- anneal at T>700 °C
  depending on implant conditions platelets or bubbles form which are nucleation sources for misfit dislocations



Strain Relaxation by X-Ray Diffraction

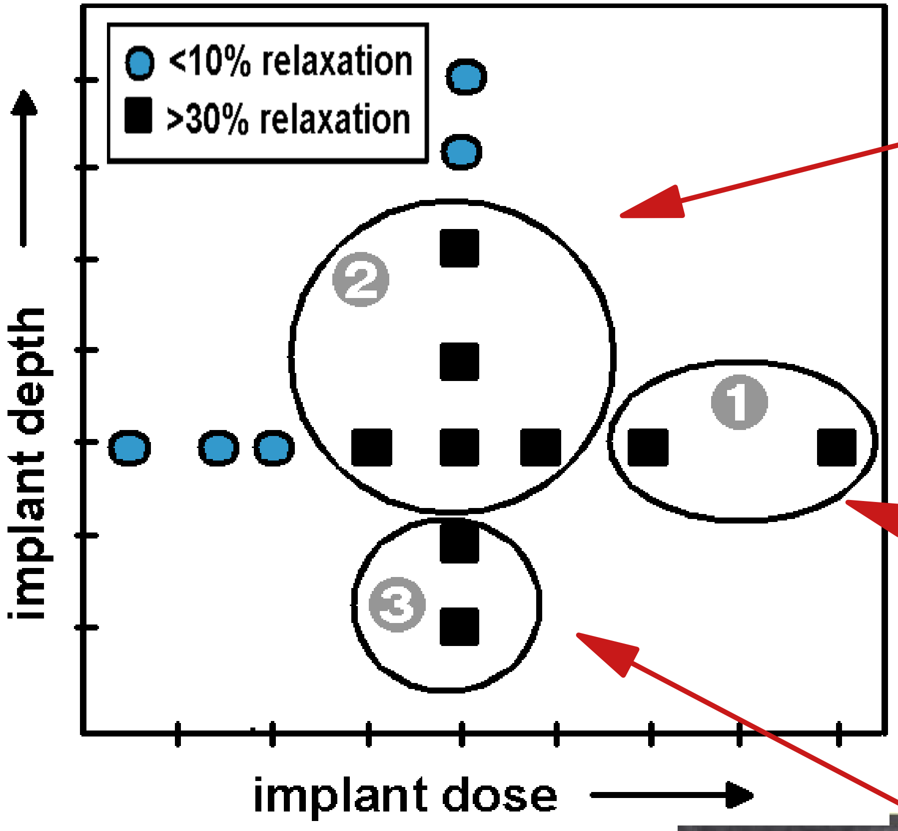
188 nm-thick $Si_{0.8}Ge_{0.2}$

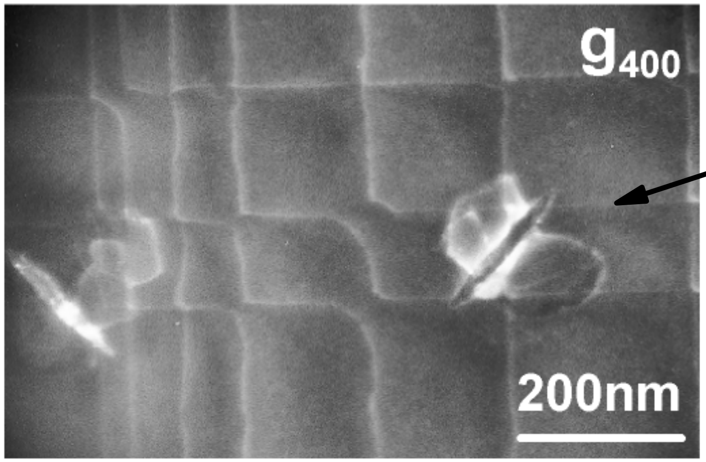




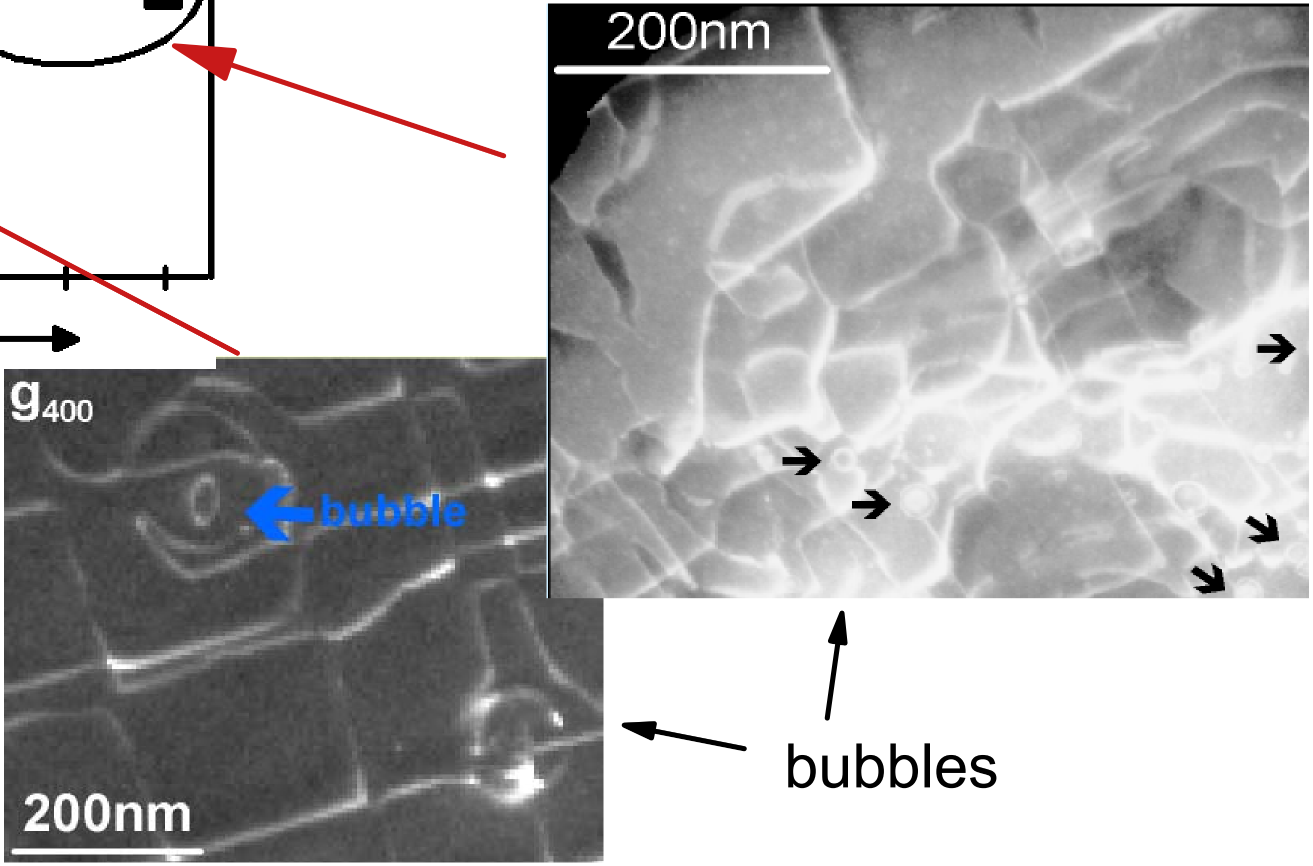
He$^+$ implantation enhances strain relaxation

Strain Relaxation Mechanisms





platelets

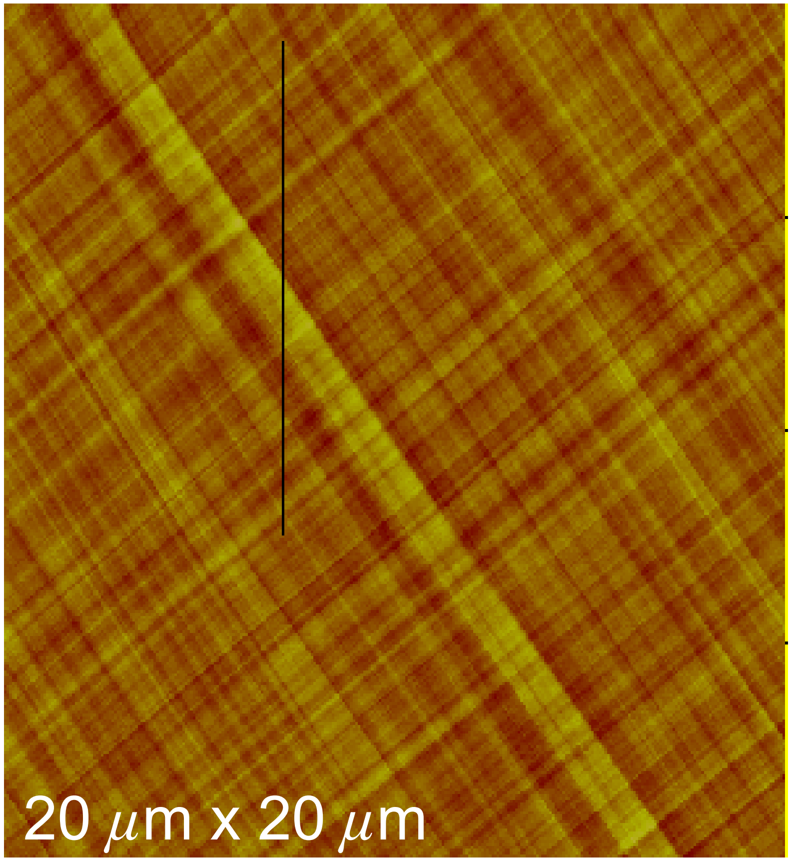


bubbles

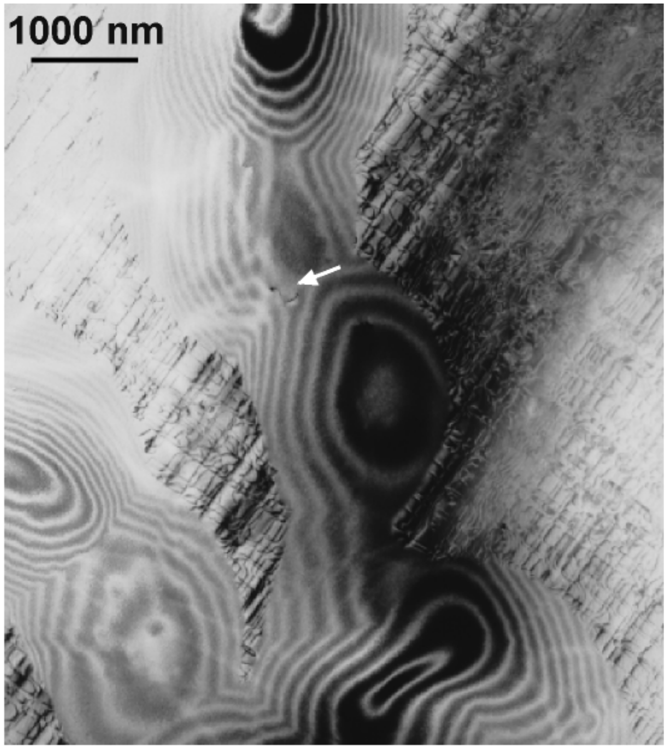
strain relaxation mechanism varies with implant conditions

S.H. Christiansen, et al. Mat. Res. Soc. Symp. Proc. **686**, 27 (2002)

Characterization of Implanted/Annealed Buffer Layers



AFM image of wafer surface
256 nm-thick $Si_{0.8}Ge_{0.2}$ layer
84% strain relaxation
RMS roughness = 0.52 nm



planar view TEM image of a 250 nm-thick, 80% relaxed $Si_{0.85}Ge_{0.15}$ layer
(arrow indicates a threading dislocation)

- threading dislocation density <5×10^{7} cm^{-2}
- defects are homogeneously distributed

SiGe-on-insulator (SGOI) substrates

Combine advantages of strained Si with SOI technology

Various approaches to get SGOI

-- oxygen implantation into thick relaxed SiGe buffer layer

N. Sugiyama, et al., Thin Solid Films **369**, 199 (2000).
T. Mizuno, et al., IEEE Elec. Device Lett. **21**, 230 (2000).

-- high temperature annealing/oxidation of SiGe

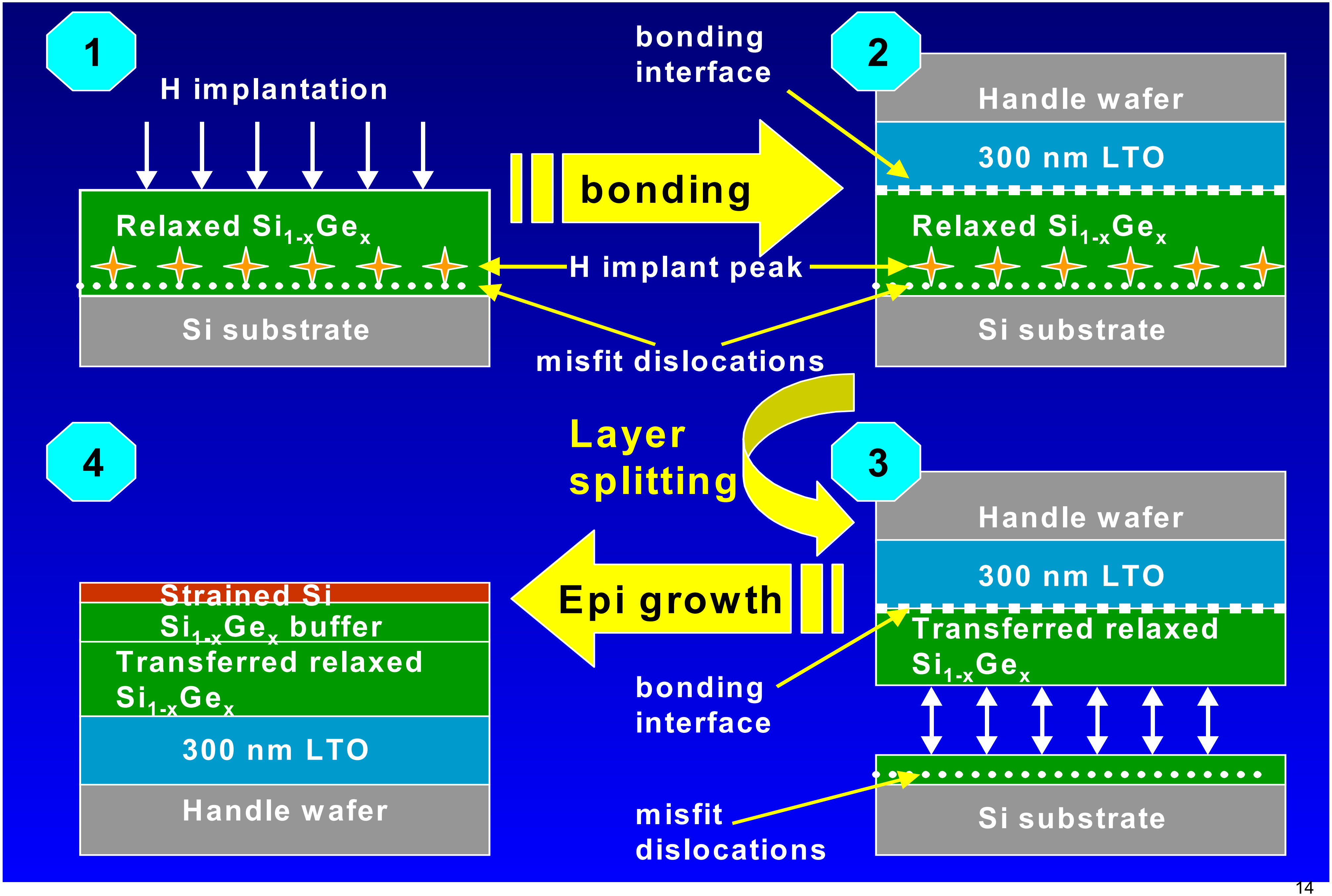
T. Tezuka, et al., Appl. Phys. Lett. **79**, 1798 (2001).
A. Sakai, et al., Appl. Phys. Lett. **79**, 3398 (2001).

-- wafer bonding and layer transfer methods

L.-J. Huang, et al., Appl.Phys. Lett. **78**, 1267 (2001).
L.J. Huang, et al., Symp. on VLSI Tech. Dig., 57 (2001).
J.O. Chu, et al., paper at the 2001 Spring MRS Meeting.
Zhi-Yuan Cheng, et al., IEEE Elec. Device Lett. **22**, 321(2001).
L. Huang, et al., IEEE Trans. Electron Devices **49**, 1566 (2002).

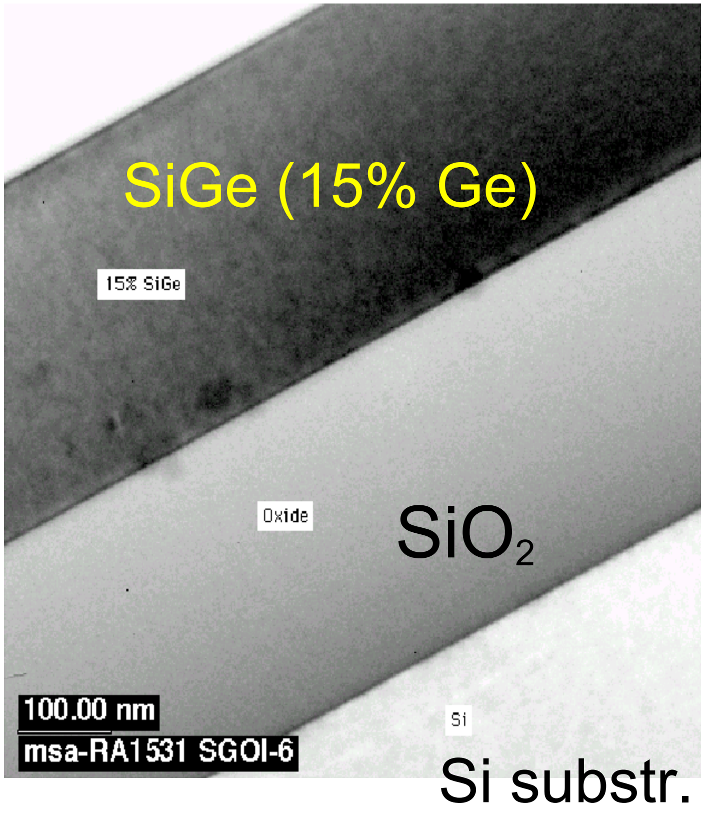
Wafer Bonding and Layer Transfer Process

L.J. Huang, et al., 2001 Symposium on VLSI Technology



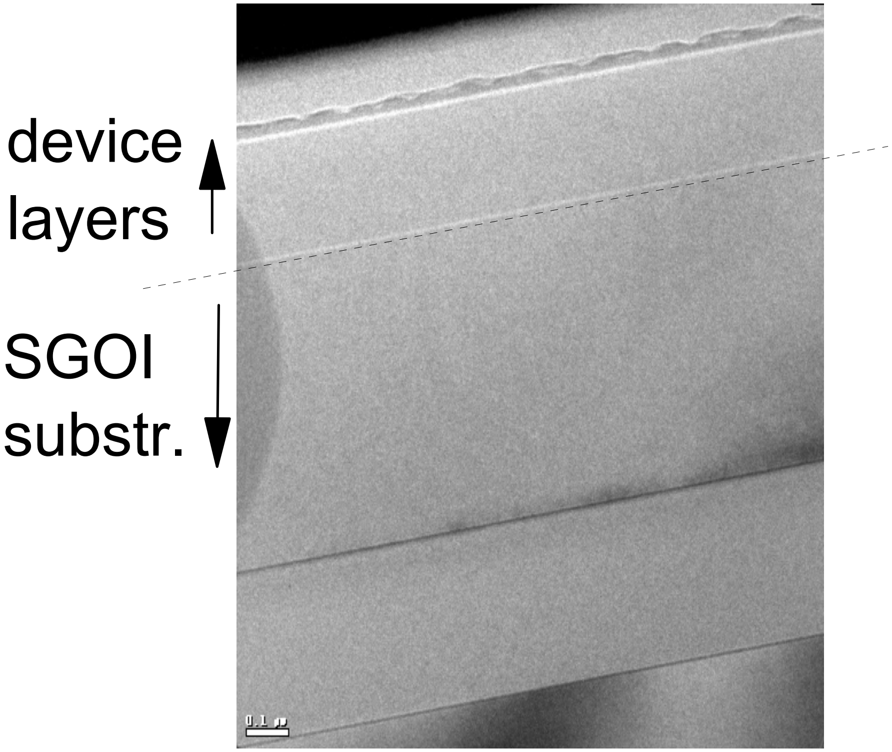
Bonded SGOI Wafers

SGOI wafer



- sucessful layer transfer

n-MODFET layer structure

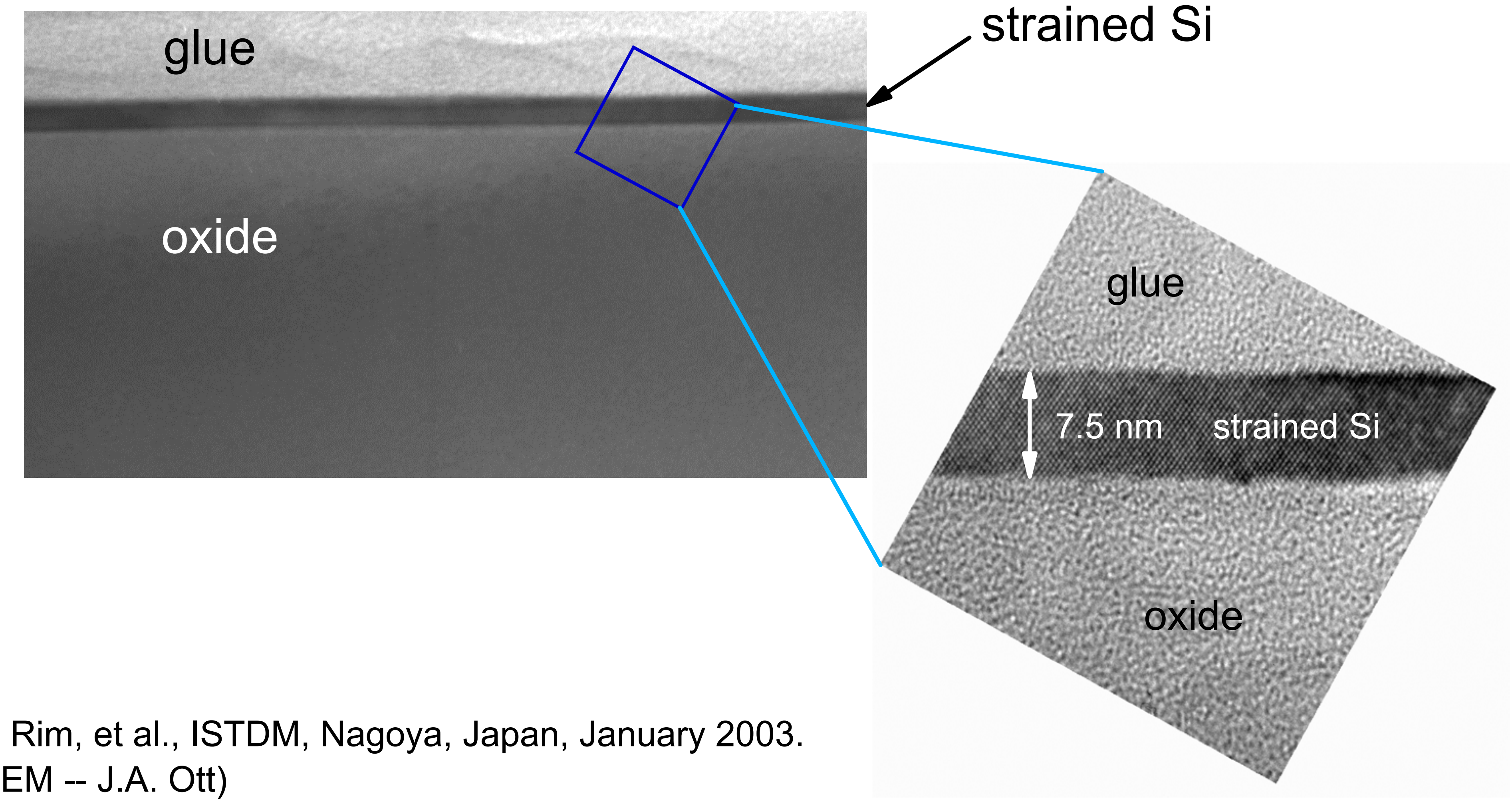


- high quality epitaxial growth on SGOI
- electron mobility same as on bulk Si

J.O. Chu, et al., Spring 2001 MRS Meeting, San Francisco

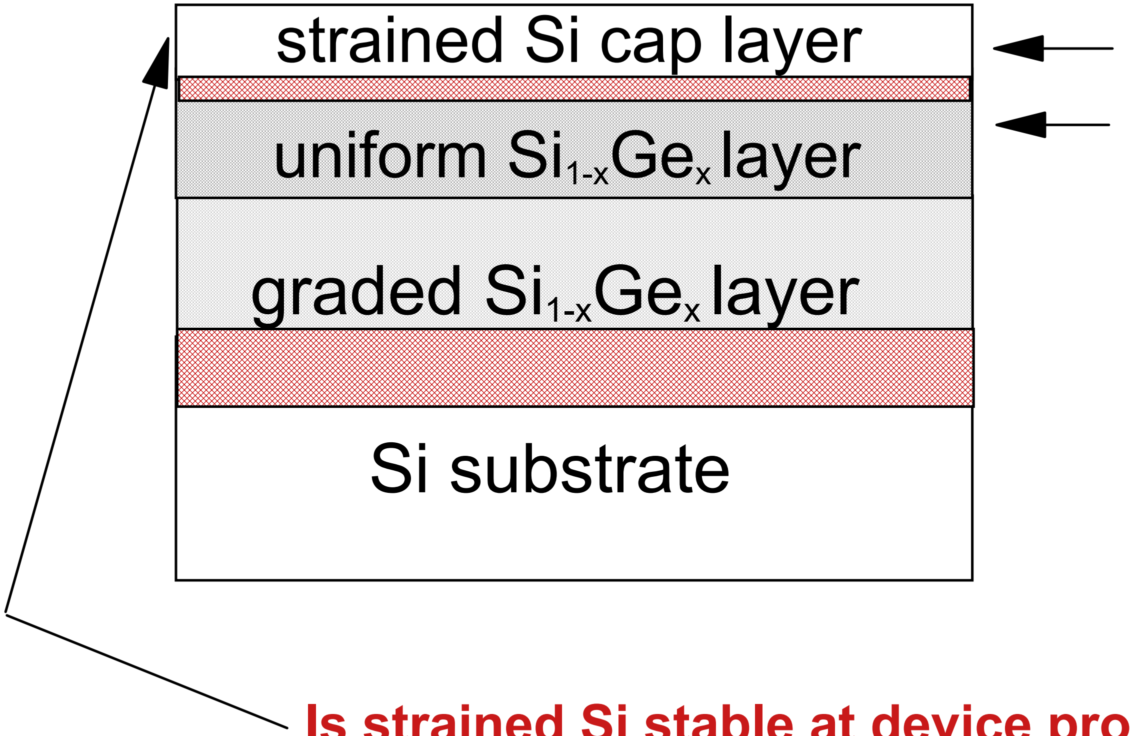
Bonded SSOI Wafer

need strained Si on oxide for future CMOS



K. Rim, et al., ISTDM, Nagoya, Japan, January 2003.
(TEM -- J.A. Ott)

Thermal Stability of Strained Si/SiGe Structures



strained Si cap layer

uniform $Si_{1-x}Ge_x$ layer

graded $Si_{1-x}Ge_x$ layer

Si substrate

cap thickness, 7-21 nm

alloy composition, $0.19<x<0.30$

rapid thermal annealing
at 1000 °C for 5-300 sec.

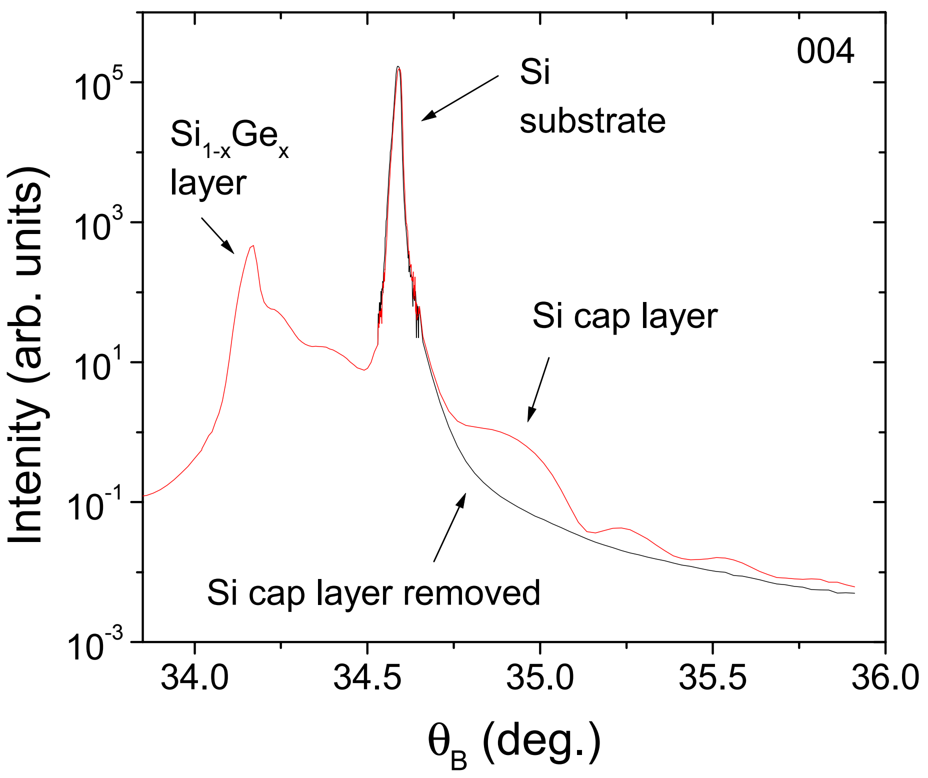
Is strained Si stable at device processing temperatures?

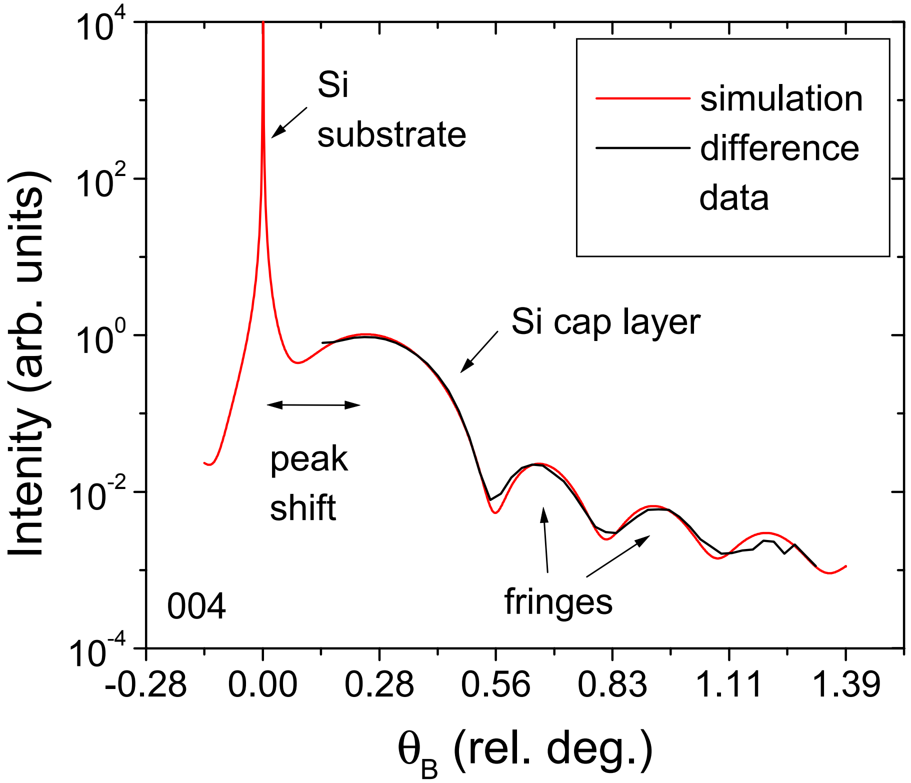
characterization methods:

- high resolution x-ray diffraction (synchrotron source)
- planar view TEM
- Raman spectroscopy (Koester, et al., APL 72, 2148 (2001))
- spectroscopic ellipsometry

X-Ray Diffraction Measurements

-- triple-axis configuration, NSLS (X20), Brookhaven National Lab
-- 004 and 224 reflections to get composition and strain of $Si_{1-x}Ge_x$ layer
-- 004 data to get thickness and strain of Si cap layer



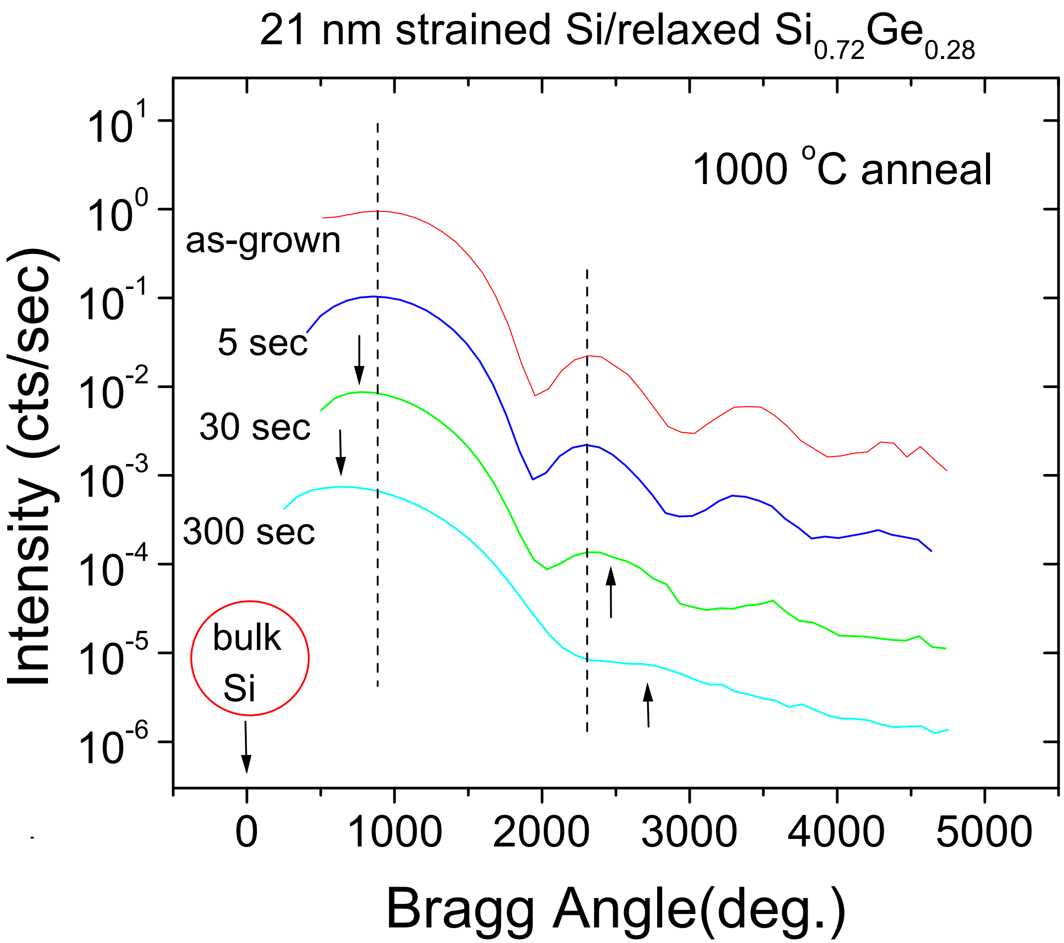


removed cap layer from some areas
took data from areas with/without Si layer

peak shift ==> strain in Si cap layer
fringe spacing ==> Si layer thickness

P.M. Mooney, et al. Mat. Res. Soc. Symp. Proc. **686**, 3 (2002)

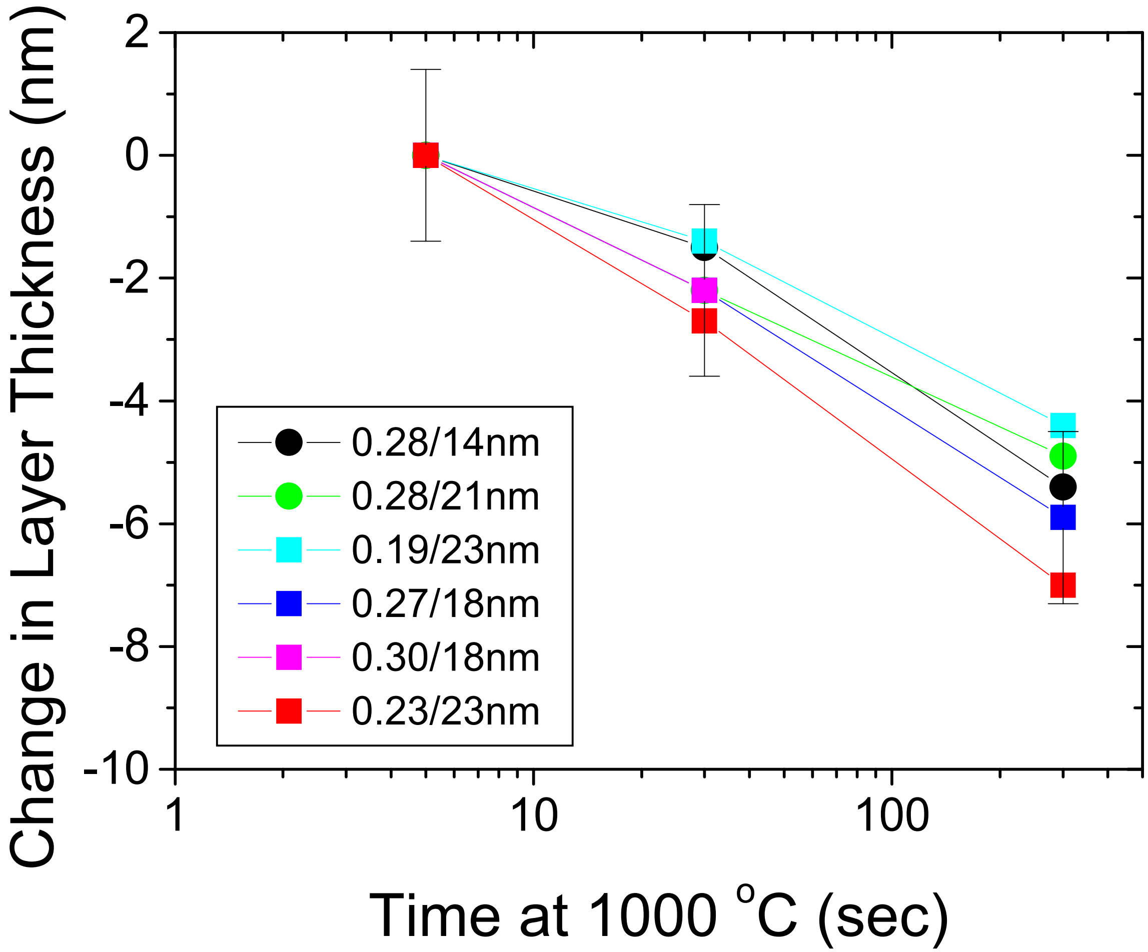
XRD Results for Annealed Wafer



note that peak shifts towards Si substrate peak and fringe spacing increases with increased annealing time

==> interdiffusion at interface and strain relaxation occur

Interdiffusion at Si/SiGe Interface -- X-ray



$Si_{1-x}Ge_x$

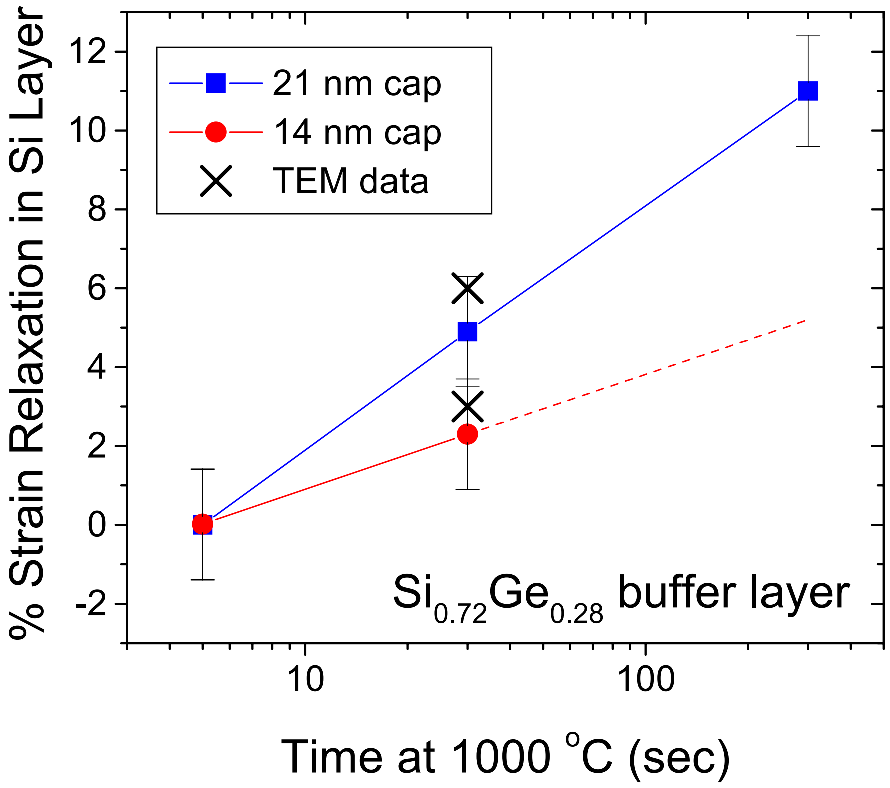
$0.19<x<0.28$

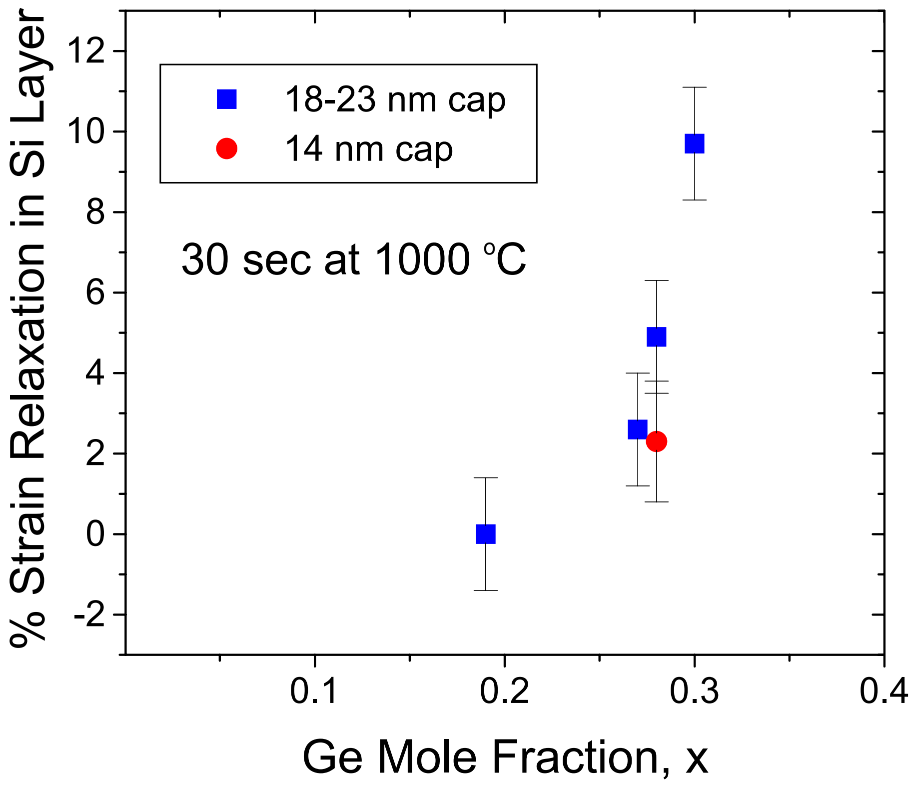
initial cap thickness
14-23 nm

-- cap thickness decreases by 2 nm (+/-1.5 nm) after 30 sec.

-- no significant dependence on alloy composition or thickness over the ranges investigated!

Strain Relaxation (XRD and TEM)





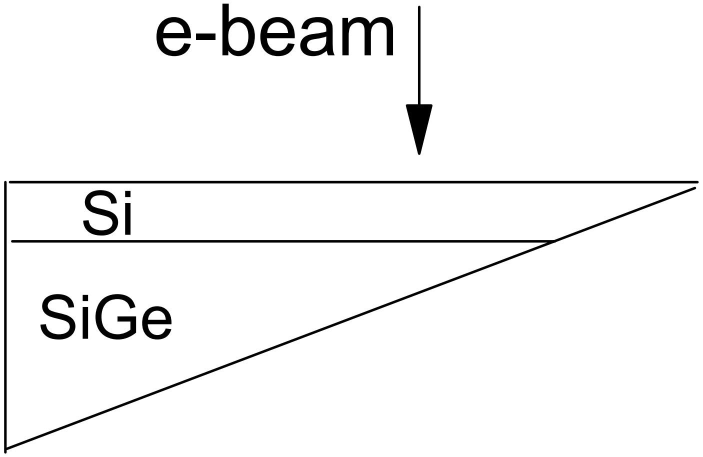
-- strain relaxation expressed as percent of initial strain

-- good agreement between x-ray and TEM results

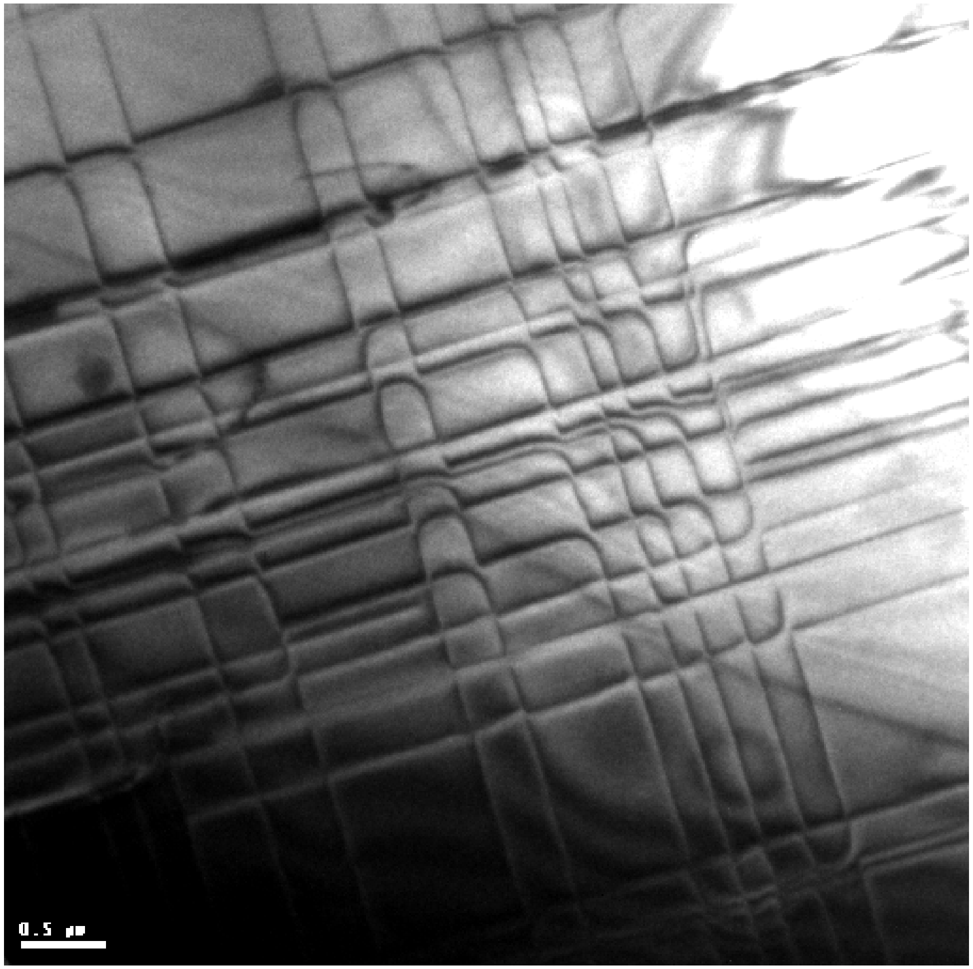
-- relaxation behavior as predicted by Matthews & Blakeslee

-- little strain relaxation occurs, but misfit dislocations are formed at Si/SiGe interface when Si layers exceed critical thickness

Planar View TEM Analysis



- look at near-surface region of the sample
- image misfit dislocations at Si/SiGe interface

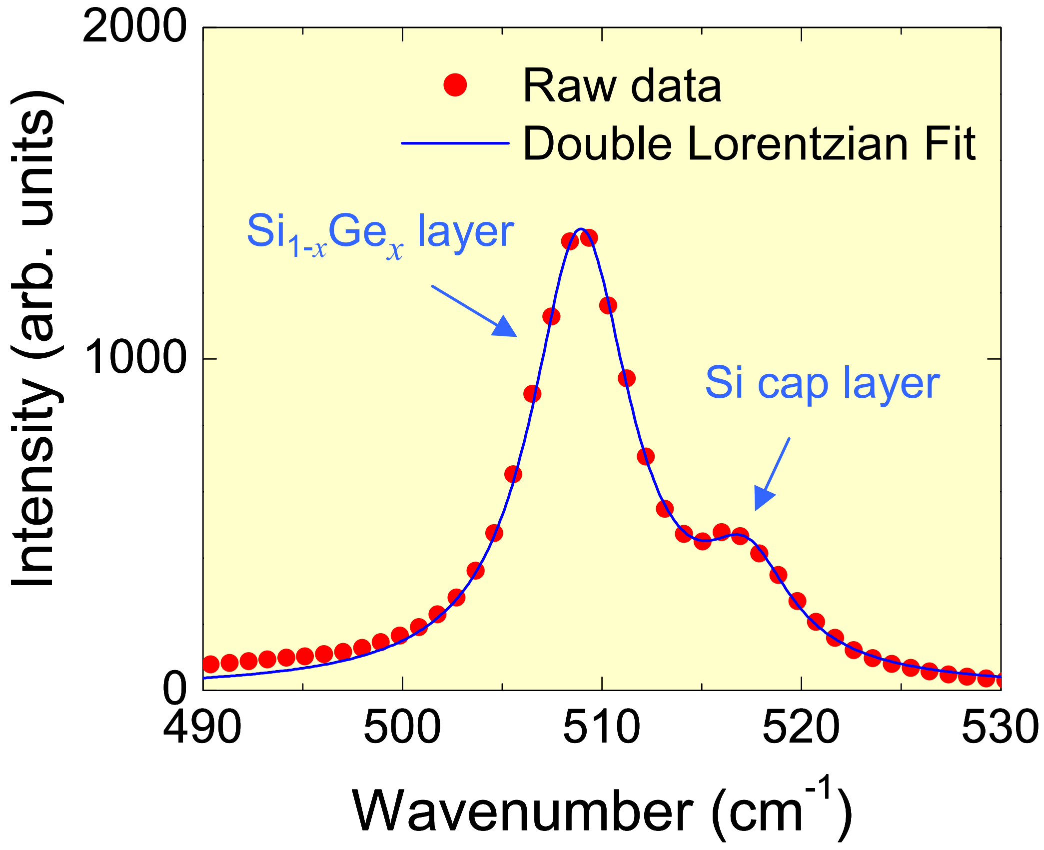


21 nm Si cap / $Si_{0.72}Ge_{0.28}$, 1000 °C 30 sec

average misfit dislocation spacing is 2.5/μm

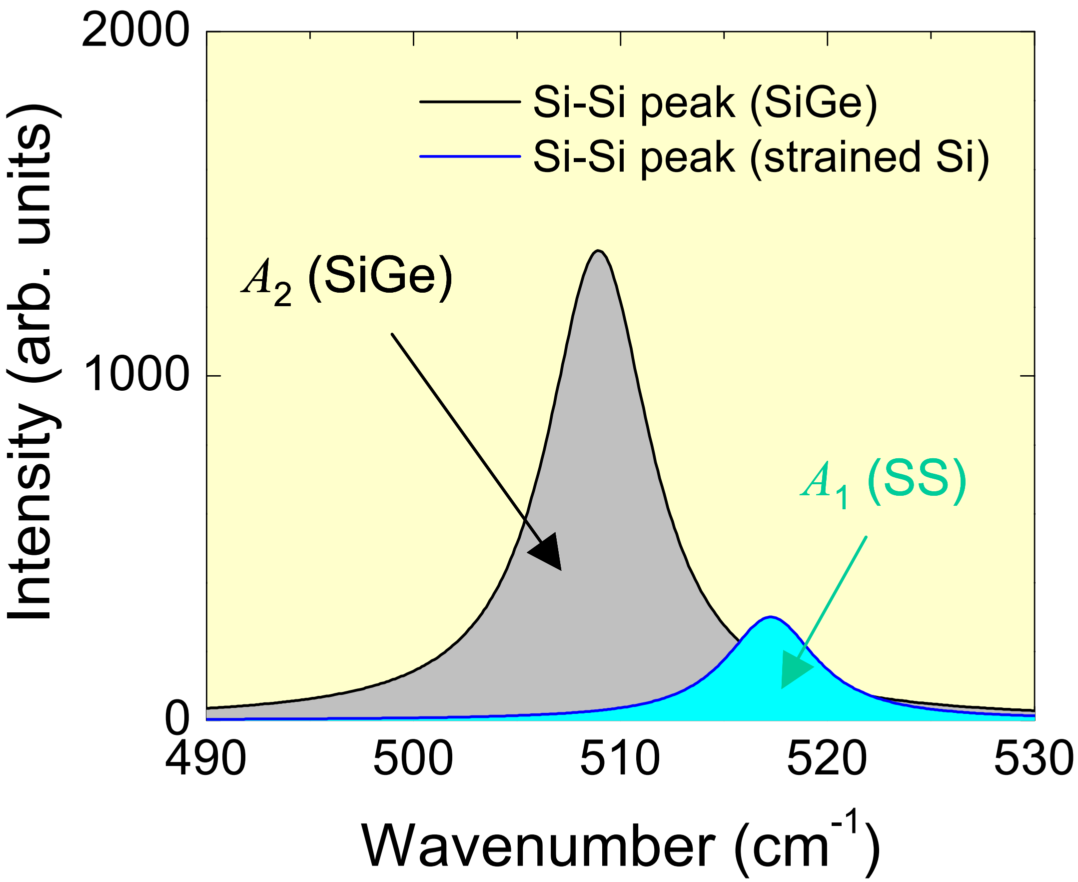
Raman Spectroscopy

- Renishaw 2000 Confocal Raman Microprobe at Miami University, Ohio,
- 488 nm excitation wavelength, 3600 mm^{-1} grating density,
- 4 mW incident power at sample.



- **Si-Si LO phonon peaks fit using double Lorentzian line shape.**

Determination of Si Thickness Change with Raman



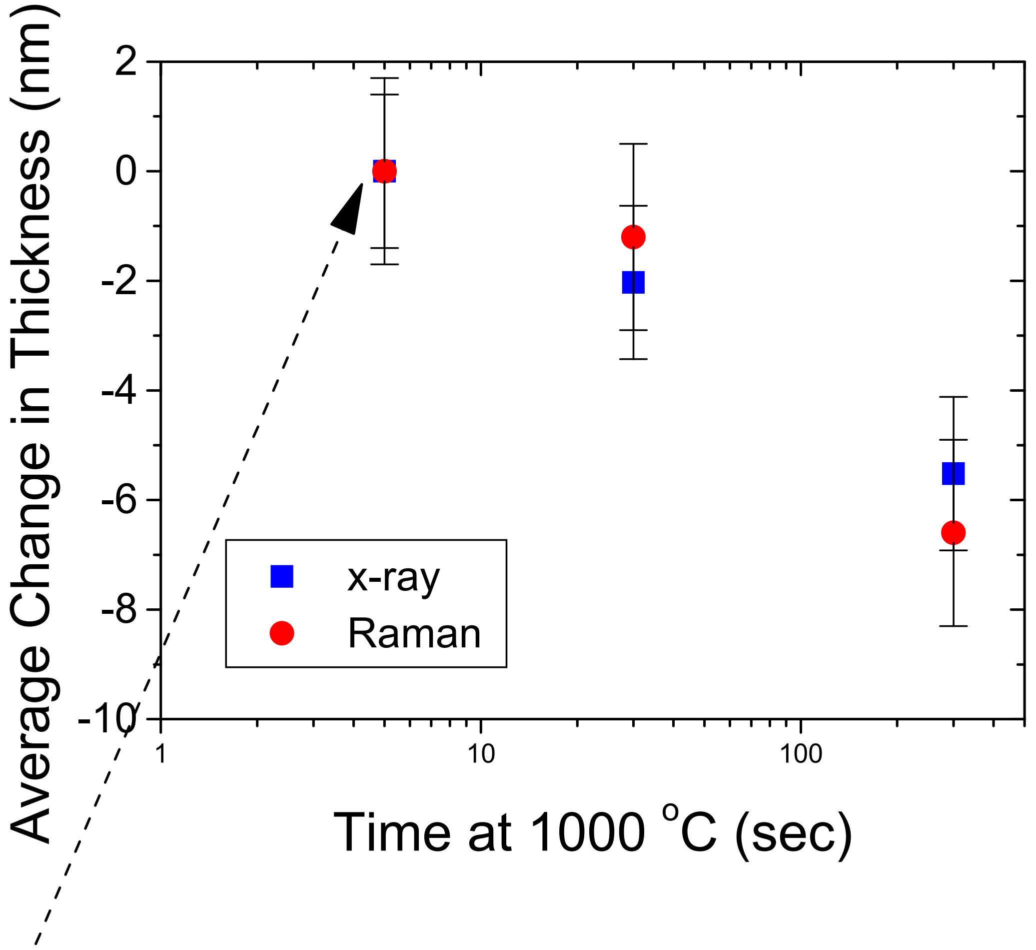
$$\Delta d_1(t) = d_{Si}(0)\cdot\left[1 - \frac{r(t)}{r(0)}\right]$$

$$where,\quad r(t) = \frac{A_1(t)}{A_2(t) + A_1(t)}$$

Determined value of $d_{\mathrm{Si}}(0)$
using HR-XRD.

- Ratio of SS and SiGe peak areas used to determine thickness of Si cap. Use HRXRD value for as-grown sample as calibration.

Comparison of XRD and Raman Results



Average values of many samples are plotted for each method.

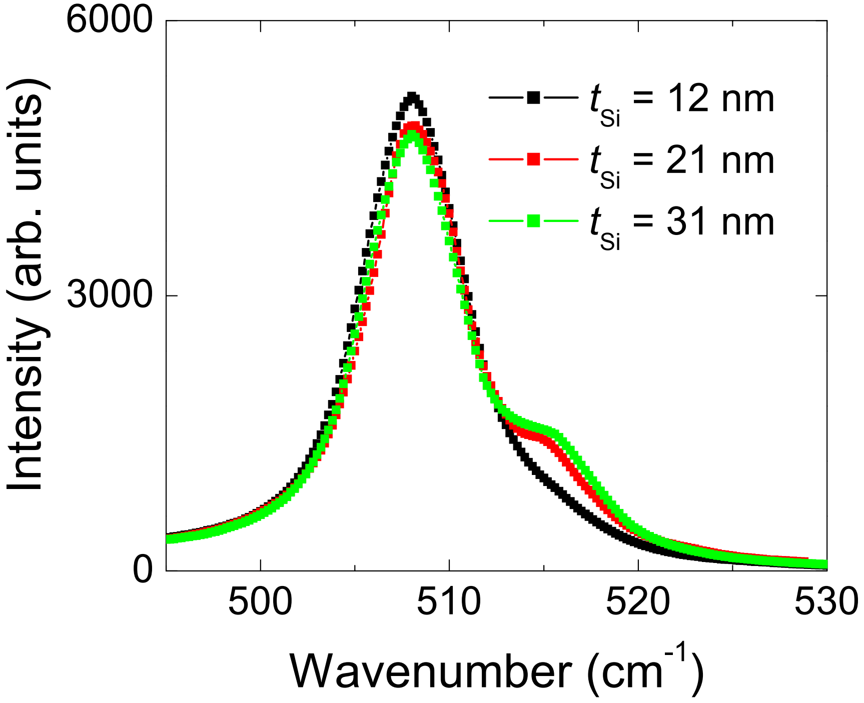
good agreement!

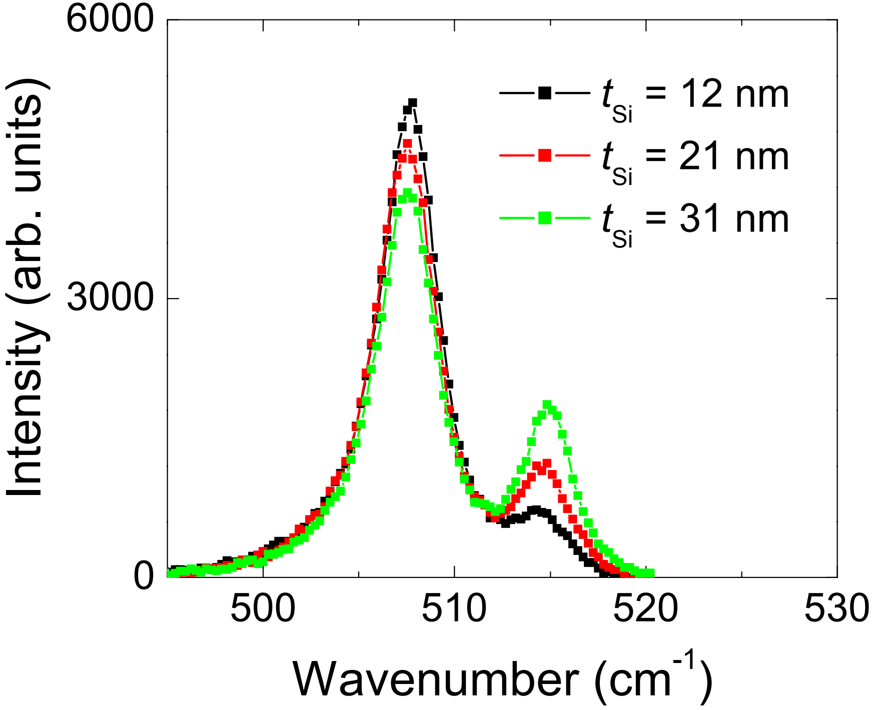
XRD values of initial layer thickness used to calibrate Raman data (488 nm)

Error bar is +/-1.5 nm for XRD and +/- 2 nm for Raman

Raman Data: Different Wavelengths

Si layers of different thickness on $Si_{0.77}Ge_{0.23}$


blue (488 nm)


violet (442 nm)

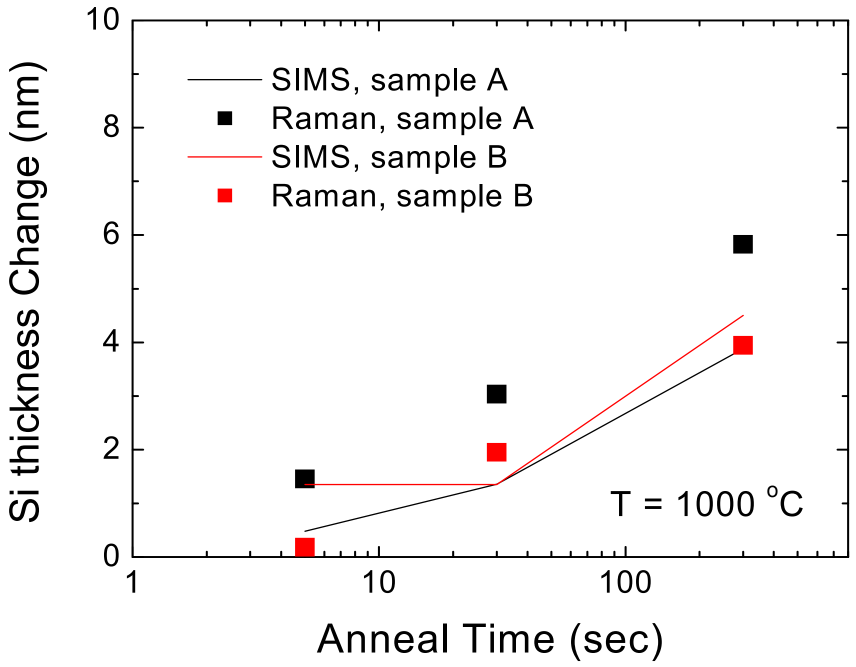
more surface sensitive at shorter wavelength

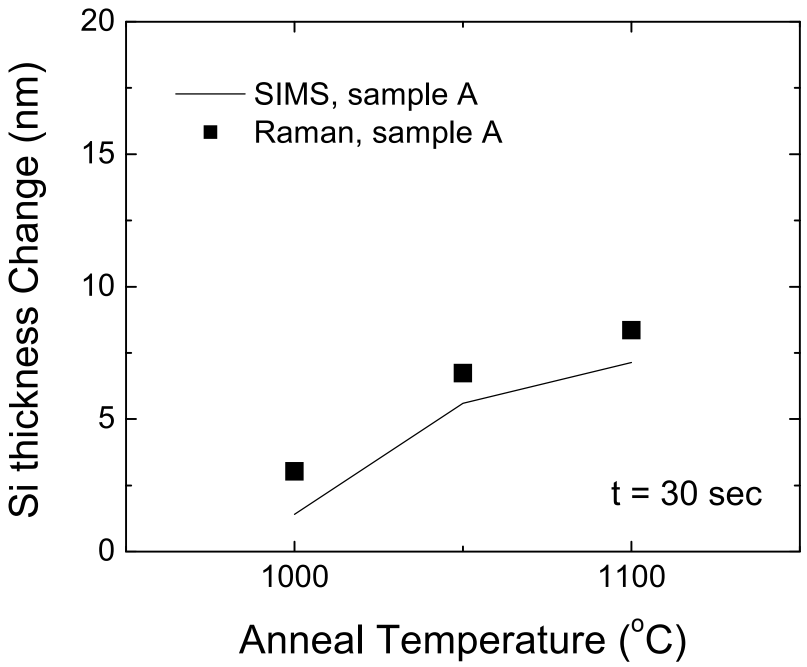
==> can detect thinner strained Si layers

on SiGe layers with lower Ge

Comparison of Raman Results (442 nm) with SIMS Data

A: 31 nm Si on $Si_{0.77}Ge_{0.23}$
B: 18 nm Si on $Si_{0.70}Ge_{0.30}$





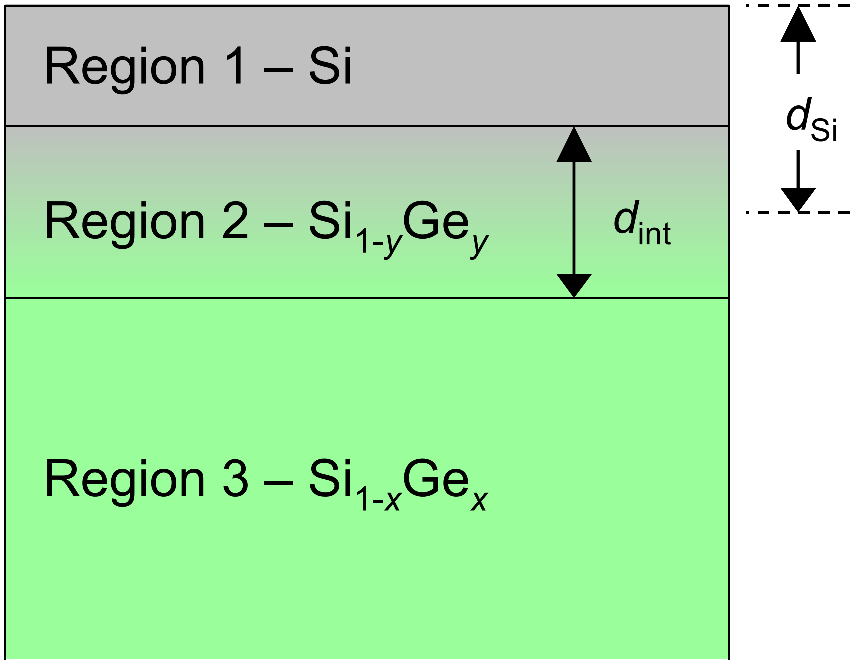
- data are consistent with earlier results
- scatter is within accuracy of measurements

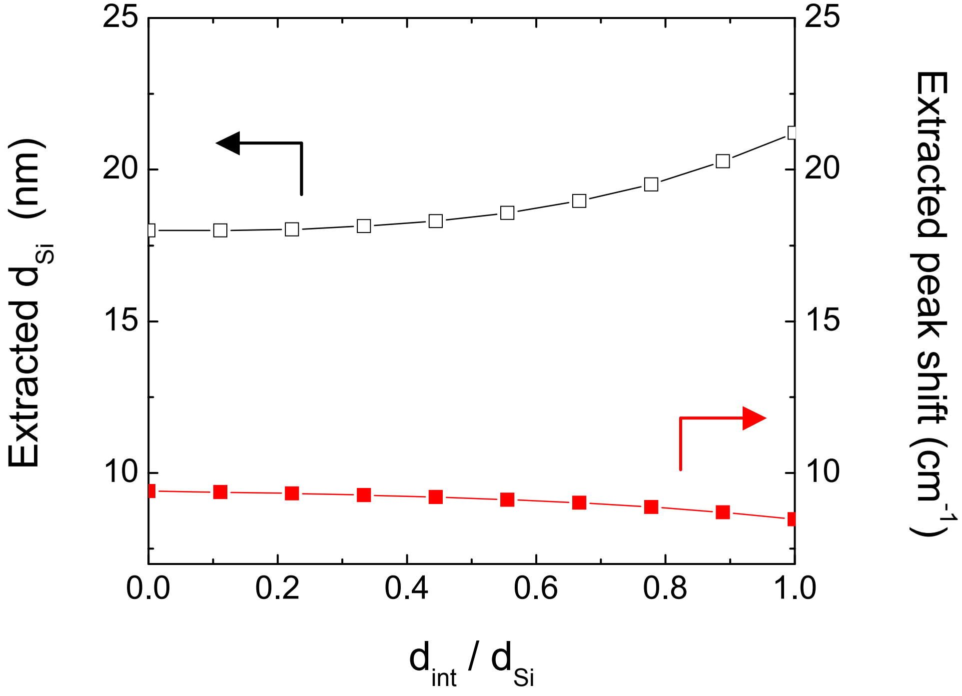
SIMS confirms that Si thickess changes by interdiffusion!

Limitations of Two-Layer Assumption

- Simulated three-layer structure, but fit with double Lorentzian.

- Varied d_{int}, while keeping d_{Si} constant. Compared extracted and input values.



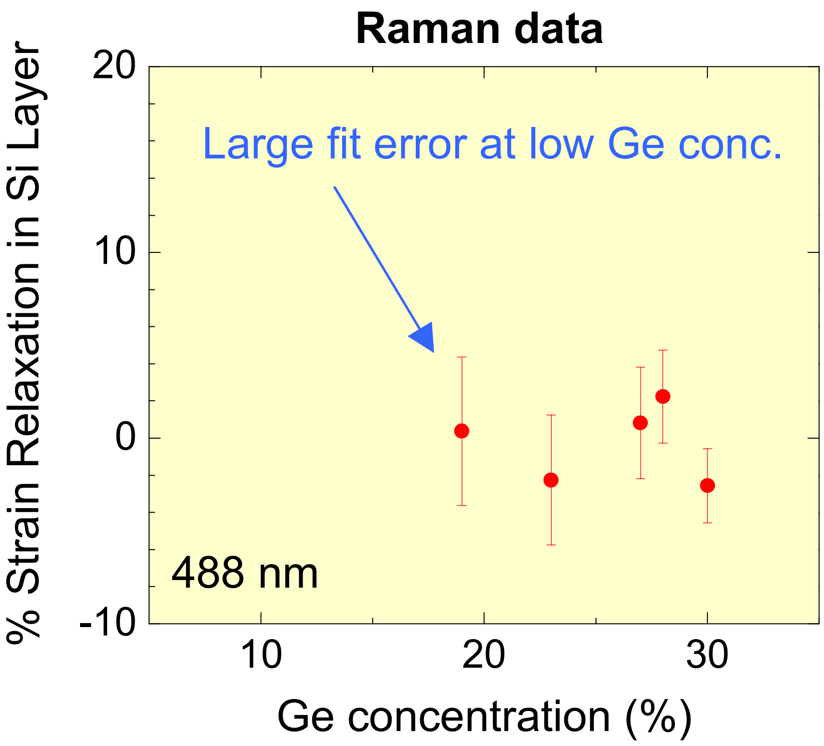


- Increaseing d_{int} causes Si peak to shift, broaden, and increase in area.

- Si thickness error > 5% when $d_{int}/d_{Si} > 0.67$. All samples in this study have $d_{int}/d_{Si} < 0.50$.

Raman Measurement of Strain in Si Layer

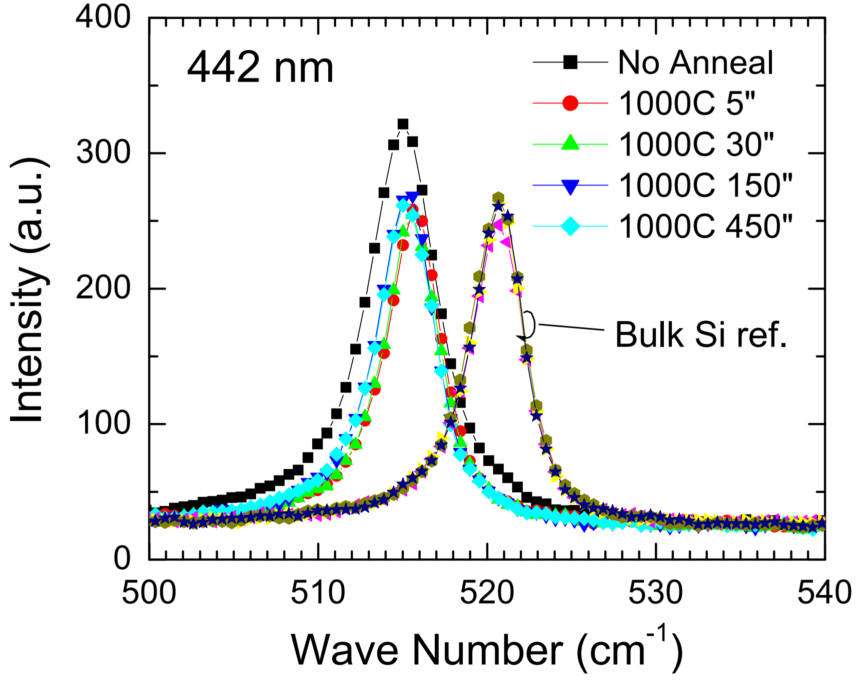
relaxation of strained Si-on-SiGe



- Uncertainty in Raman data too large to detect the small degree (<5%) of strain relaxation in Si/SiGe samples!

S.J. Koester, et al., Device Research Conference, Santa Barbara, June 2002.

strained Si-on-insulator



- Strained Si layer transferred by wafer bonding
- Compare strained Si layer with bulk Si
- Si layer remains strained after annealing

K. Rim, et al., ISTDM, Japan, January 2003.

Spectroscopic Ellipsometry

- proven method for characterization of dielectric films
- best results when there is a significant difference in k and n between materials
  - e.g. oxide or nitride on Si, SOI, SGOI, SSOI
- requires many parameters to model structures having several layers
  - need good values for optical constants for each material

- useful for thickness of strained Si on relaxed SiGe??
  - poor results for graded buffer layers -- better for strained Si layer than for SiGe
    - surface/interface roughness?
    - poor optical data for dislocated SiGe layers?
  - reasonable results for strained Si on implanted/annealed buffer layers

example:	- TEM	7.2 nm	
	- XRD	7.9 nm	agreement is within uncertainty
	- ellipsometry	6.5 nm	of XRD measurement!

- what accuracy is needed??

Conclusions

Enhanced electron and hole mobility in strained Si devices demonstrated

-- standard fabrication processes, 200 mm wafers

Materials/Structures

-- graded buffer layers are standard

>90% relaxation at any alloy composition

-- implanted/annealed buffer layers

thinner/smoother surfaces than graded layers

-- insulator substrates fabricated by wafer bonding methods

SGOI and SSOI

Nondestructive characterization methods

-- x-ray diffraction good for composition/strain of SiGe layers, but strained Si cap layer is difficult

-- Raman spectroscopy is good for strain in SSOI, but strained Si on SiGe is difficult & need calibration to measure Si thickness

-- spectroscopic ellipsometry useful to measure layer thickness for SGOI and SSOI -- further work needed for structures with many layers, but likey to be useful for strained Si on SiGe